IN THE SPECIFICATION:

Please add the following new paragraph after paragraph [0018]:

[0018.1] Figure 4 is a timing diagram illustrating the operation of a buffer circuit according to an embodiment of the invention.

Please add the following new paragraphs after paragraph [0032]:

[0032.1] A timing diagram illustrating the relationship between the signals of the above-described buffer circuits is illustrated in Figure 4. For example, the assertion of the pulse by the further AND gate 55, via its output A55, is illustrated at time T6. As stated above, the further AND gate 55 is fed signal A53, the inverted version of the signal A51 and the clock signal CLK. Accordingly, when A53 and the CLK are a "1", and A51 is a "0", the further AND gate 55 outputs a "1", thus asserting the pulse. This is illustrated by arrows 406, 408 and 410, respectively.

[0032.2] Another timing relationship illustrated in Figure 4 is the resetting of the edge-triggered RS flip-flop 53. This is illustrated at time T7. As stated above, the edge-triggered RS flip-flop 53 is reset when the output signal A54 of the third AND gate 54 is a "1". This is shown by arrow 416. In order for the third AND gate 54 to output a "1", both the inverted version of the clock signal CLK and the inverted version of the signal A51, must be "0". This is illustrated by arrows 412 and 414, respectively. In contrast, if either the CLK or A51 is a "1", the third AND gate 54 will output a "0". This is illustrated by arrows 402 and 404 at time T2, where, the CLK and A51 are both "1".